REMARKS

The Examiner is thanked for the Office Action. Claims 1,4-22, and 24-38 are currently pending in the present application. All claim rejections are hereby respectfully traversed. Favorable reconsideration is respectfully requested.

The Examiner has rejected claims 1 and 4-8 over Lentz (USPN 5886705, Young (5831637), Tanaka (579371), Saunders (6046747), and Chimoto (5550961). Claim 1 is reproduced for purposes of discussion.

> 1. A graphics accelerator for processing a graphical image, the graphics accelerator comprising:
>
> a single texture buffer for storing texture maps and data relating to the texture maps stored in the texture buffer; and
>
> a plurality of texture processors that perform texturing operations on the graphical image, the plurality of the texture processors retrieving texture packets from the single texture buffer,
>
> each texture processor including a fetching engine that retrieves the texture packets, each texture packet being stored in the texture buffer and being associated with a texture map that is different than the texture maps associated with any other texture packet in the texture buffer, each texture packet including data relating to the location of its associated texture map in the texture buffer and data relating to the dimensional type of that texture packet's associated texture map.

Examiner addresses Applicant's previous arguments at page 2 of the current Office action, stating:

> The number of references is questioned by Applicant at pages 4-5, however, the number of references does not weigh against the obviousness of the claimed invention. In re Gorman.

I. One of ordinary skill in the art would not have made the combination proposed by the Examiner, since the references themselves contain no suggestion--explicit or implicit--to make the proposed combination.

The MPEP states,

> reliance on a large number of references in a rejection does not, without more, weigh against the obviousness of the claimed invention. See *In re Gorman*, 933 F.2d 982, 18 USPQ2d 1885 (Fed. Cir. 1991).

[Emphasis added.]

This passage appears to note that a large number of references doesn't necessarily equal nonobviousness; however, it also suggests that the number of references cited can, when there is other evidence, weigh against the obviousness of an invention. This is explicitly stated in Gorman ("without more").

In the present case, Examiner has selected elements from five different references to reject the present innovations. However, it is respectfully submitted that several of these references do not appear to teach what Examiner suggests. These flaws in the references, which are discussed below, combined with the sheer number of references that were combined, do in fact weigh against the obviousness of the claimed invention. Further, there is no teaching or suggestion in the art to make the very selective choices Examiner has made from the various references in order to argue the claimed invention is obvious. Gorman itself discusses the limitations on combining references:

> When it is necessary to select elements of various teachings in order to form the claimed invention, we ascertain whether there is any suggestion or motivation in the prior art to make the selection made by the applicant. Interconnect Planning Corp. v. Feil, 774 F.2d 1132, 1143, 227 U.S.P.Q. (BNA) 543, 551 (Fed. Cir. 1985). "'Obviousness can not be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive

> supporting the combination.'" In re Bond, 910 F.2d 831, 834, 15 U.S.P.Q.2D (BNA) 1566, 1568 (Fed. Cir. 1990) (quoting Carella v. Starlight Archery and Pro Line Co., 804 F.2d 135, 140, 231 U.S.P.Q. (BNA) 644, 647 (Fed. Cir. 1986)).
>
> The extent to which such suggestion must be explicit in, or may be fairly inferred from, the references, is decided on the facts of each case, in light of the prior art and its relationship to the applicant's invention. As in all determinations under 35 U.S.C. § 103, the decisionmaker must bring judgment to bear. It is impermissible, however, simply to engage in a hindsight reconstruction of the claimed invention, using the applicant's structure as a template and selecting elements from references to fill the gaps. Interconnect Planning, 774 F.2d at 1143, 227 U.S.P.Q. (BNA) at 551. The references themselves must provide some teaching whereby the applicant's combination would have been obvious.

[Emphasis added.]

Applicant therefore respectfully submits that one of ordinary skill in the art, if confronted with the problem of reducing command bandwidth of texture maps, would not have been motivated to make the particular selections from the cited references--none of which actually solves the problem addressed by the present application, in the way it is solved by the present application. It is respectfully submitted that, without the present claims as a template, one of ordinary skill in the art would not have found the present innovations obvious, in light of the cited references.

Examiner also mentions the motivation for making the proposed combination, stating:

> the motivation given by the examiner of more rapid processing is a goal of one skilled in the computer graphics field in order to better computer generated images.

Applicant respectfully submits that stating a general goal (faster computing) is not a motivation to make the specific combination of elements, selected from the five different references, that Examiner asserts. "It is

impermissible within the framework of section 103 to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art." *In re Hedges*, 228 U.S.P.Q. 685, 687 (Fed. Cir. 1986). [Emphasis added.]

It is therefore respectfully submitted that the examiner uses impermissible hindsight, relying on the present claims themselves as a template, in order to determine what elements from the various prior art references to select and combine in rejecting the claims. There is no teaching or suggestion in any of the references to make the proposed combination, whether explicit or implicit. Further, making the proposed combination would significantly modify the functioning of any of the cited references, so that they themselves would no longer function as described.

When such departure from the teaching of a references is needed in making a combination for obviousness, it is respectfully submitted that the combination is not obvious, especially when elements must be selectively spliced together from no less than five different references, combined to form an invention that functions as none of the references do themselves.

II. Flaws in the Examiner's interpretation of the various references:

A. Lentz does not appear to teach the use of texture packets; it is directed toward a different problem than the present claimed invention; and it uses different techniques to solve the problem that it does address.

Examiner cites Lentz, stating,

> Lentz discloses...the plurality of the texture processors retrieving texture packets from the single texture buffer (See Abstract, Fig 1, Fig 2, col. 1 lines 5-13)

Applicant respectfully submits that Lentz does not appear to teach the use of texture packets.

The cited text, column 1, lines 5-13, state:

> The present invention is directed to texture mapping in computer graphics. It specifically concerns the manner in which a texture image is stored for use in texture mapping.
>
> A situation commonly encountered in computer graphics is the need to render an image of an object whose surface has a detailed pattern. The surface's image is computed from digital samples of the pattern itself. That stored pattern image is known as a texture map.

The cited passage generally mentions texture mapping and rendering, but does not mention texture packets. The term "texture packet" does not appear in the text of Lentz. Lentz is directed to rearranging MIPMAPs into DRAM friendly blocks. Its main focus is on minimizing memory page changes, as stated at col. 3, lines 30-36:

> Although the resultant address computation is more complicated than, for instance, that of the mip-map organization described above, my approach can yield greater speeds, since it minimizes the occurrence of memory-page changes, which I have recognized are a greater obstacle to high-speed texture data removal than address computation is.

Lentz achieves this by innovatively arranging blocks of texel data into corresponding memory blocks:

> In accordance with my invention, the texture space is divided into a plurality of regions, the texture memory is divided into a plurality of corresponding memory blocks, and a single memory block contains all of the different-spatial-resolution texture maps' texel data representing the same, corresponding texture region.

Hence, Lentz is not directed toward the problem addressed by the present innovations, and it solves the problem that it does address using different techniques than described in the present claims.

B. Tanaka's packet data is for commands, not for abstracting texture data. Meanwhile, the present invention removes the need for the information to be held in the command packet. Tanaka does not achieve this.

In rejecting claim 1, Examiner refers to Takana:

> The combination of Lentz and Young do not explicitly disclose that a texture packets identifying the location of a texture map. However, Tanaka et al clearly discloses that the packet data, which represents the storage location of a texture data/map. (See col. 2, line 55-62, col. 8, line 26-34).

It is respectfully submitted that the "texture packet" of Tanaka is a command packet, produced by the processing action of the coordinate transforming device. This packet data does not appear to be stored in the texture buffer. However, the "texture packet" of the present innovations is not a command packet, and is stored in the texture buffer. None of the references cited by Examiner appear to teach or suggest storing the texture packet of the claimed inventions in the texture buffer. Examiner seeks to cure this deficiency by citing Young, discussed below.

C. Young does not appear to teach a texture packet is stored in the texture buffer; particularly, Young does not teach or suggest the texture packet of the present innovations (which are associated with a texture map and which include data relating to the location of the associated texture map in the texture buffer) being stored in the texture buffer.

Examiner appears to cite Young as teaching the claimed limitations of, "each texture packet being stored in the texture buffer...." in the context of at least claim 1.

However, Applicant finds no teaching in Young that a texture packet, as claimed, is stored in the texture buffer, in the context of claim 1.

Further, none of the cited references appears to teach the texture packet, containing the data of the claimed texture packets, <u>being stored in the texture buffer as claimed</u>.

If Applicant has overlooked a relevant teaching, it is respectfully requested that such teaching be pointed out with particularity.

D. Saunders teaches optimizing display lists with the CPU to avoid repeatedly leading texture maps; this is not the same as reducing the command bandwidth required to use a texture (by means of the present innovations), which Saunders does not address.

Examiner cites Saunders:

> The combination of Lentz, Young, and Tanaka do not specifically disclose that texture packet has data relating to the dimensional type of its texture map. However, in an analogous art (texture mapping), Saunders et al discloses that "the special bind texture call includes a target parameter that <u>defines the dimension of the texture map</u> and an ID number that identifies the display list texture object.

Applicant respectfully submits that merely defining the dimension of a texture map in the parameter of Saunders does not teach or suggest the claimed limitations of the present claim, specifically, "each texture packet including data relating to the location of its associated texture map in the texture buffer and data relating to the dimensional type of that texture packet's associated texture map," as claimed in claim 1. It is respectfully submitted that Examiner has selected an aspect of Saunders, taken it out of its context in Saunders, and combined it with other elements from the various references without

motivation or suggestion from any of the references. Further, Saunders only teaches a call to get the dimensional data, and does not teach or suggest that the dimensional data is stored in a texture packet as described in the present innovations. Saunders states, as cited by Examiner at col. 6, lines 56-67:

> The display list texture object list is used for quickly identifying optimized textures. In step 154, a special bind texture call that references the display list texture object is inserted into the display list. <u>The special bind texture call includes a target parameter that defines the dimension of the texture map and an ID number that identifies the display list texture object.</u> The effect of these operations is that, when the texture map corresponding to a glTexImage command is determined to be optimizable, a bind texture call is substituted for the glTexImage command or commands in the display list. The bind texture call references the display list texture object containing the required texture information.

[Emphasis added.]

This passage of Saunders appears to suggest that "target parameter" of Saunders (which examiner is equating with the texture packet of the present innovations because it defines the dimension of the texture map) is not stored in the texture buffer, but is instead "inserted into the display list." <u>This specifically teaches away from a texture packet having the dimension of the texture map being stored in the texture buffer.</u>

Saunders addresses the problem of optimizing display lists with the CPU to avoid repeatedly loading texture maps. However, this is not the same as reducing the command bandwidth required to use a texture, which is an advantage and result of the present innovations, and which notably is not an advantage of the Saunders teaching. In Saunders, the texture object that the Examiner refers to is part of a software linked list structure holding texture map information. The present innovations thus move from a CPU controlled software data structure to automatic handling of texture objects in hardware. This change is not addressed in Saunders (nor in any of the cited references). It is therefore respectfully submitted that even if Saunders is properly combined

with the other references, the proposed combination does not teach or suggest all limitations of the present claim 1.

The arguments presented above describe Applicant's respectful submission of flaws in Examiner's interpretation of the cited references. Because these references are also cited against independent claims 9, 15, 21, 26, 29, 32, 35, it is respectfully submitted that all independent claims are distinguished from the cited references.

Further, by virtue of their dependence on allowable claims, all dependent claims are also believed distinguished from the cited references. Favorable reconsideration is respectfully requested.

Docket No.

Conclusion

Thus, all grounds of rejection and/or objection are traversed or accommodated, and favorable reconsideration and allowance are respectfully requested. The Examiner is requested to telephone the undersigned attorney or Robert Groover for an interview to resolve any remaining issues.

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Respectfully submitted,

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